

Detector Chips

Detector chips fall into the category of imagers for cameras (CCD or CMOS), Infra-red cameras, optical disk read heads, or X-Ray imaging for medical, astronomy, or baggage scanning systems. Typically photons are collected by a detector, while these chips perform the amplification and readout functions. In visible wavelength or near infra-red imaging, the detectors are integrated directly onto the silicon chip.

Radiation Detector Readout Chip for Mars Science Laboratory

This chip will go into the MSL RAD instrument. The rover is expected to launch in 2009.

Circuit Features

- Selection of shaping time constants. There are 16 selections.
- Power down enable/disable per channel.
- Test signal input bussed to all channels, individual enable switch at each channel to connect test signal bus to input of channel.
- Selectable gain adjustment, 1x, 2x, 4x, & 8x per channel.
- Two signal paths, one with a comparator and one with a slow shaper filter followed by another comparator and a peak hold circuit.
- Two adjustable threshold DACs, one for each path (8-bit).
- Peak hold circuit for slow path.
- Dummy channels at each end of the array to maintain uniformity. These channels are fully functional but have internal nodes wired out as test pads to observe the circuit functionality in more detail.
- Capability to monitor in continuous mode the peak hold output of any given channel. With peak hold circuit is in follower mode. (for diagnostic use).
- Low-EMI signaling on all digital interfaces which must switch during signal acquisition, e.g., trigger, readout-initiate, reset.
- Ability to wire several chips with simple scheme connected to a single controller.
- Generalization of the “neighbor” readout mode using high-speed hit/read register to send hit pattern to and receive read pattern from external controller (FPGA). Sparse mode to work by default if no manipulation of the hit/read register is made during readout.
- Differential analog output (with disable) to allow connection between one or more ASICs and AD92xx or similar type A/D converters with only a unity gain buffer. Separate enable pin to reduce power dissipation when not needed.
- Single ended analog output with 2V range.
- Peak hold circuit enabled upon any fast path trigger
- Radiation tolerant layout techniques consisting of increased N+ diffusion spacing and guard rings throughout.

Other channel specifications

Channel to channel matching for channels in the same chip set to the same settings	At input to comparator +/- 200mV for 2 sigma.
Channel to channel crosstalk	0.1% target
Temperature range	-55C to +90C
Signal linearity (input charge size to voltage output)	+/-10%
Power supply	5V +/- 10%
Power dissipation per channel	7mW maximum
Channel noise level	0.3mV rms maximum at output of shaper for 4.5us peaking time setting. This is the RMS sum of the buffer input and shaper together
Chip output noise level	0.4mV rms maximum at output of single ended analog buffer in 4.5us peaking time setting. Due to noise from all circuits within the chip
Effects of Temperature variation	Gain: 2000 ppm/C Linearity: 1% over bottom half of temp. range Threshold: <1mV over full temp. range (referenced to input) Offset (baseline shift): <1mV over full temp. range

18 Channel X-Ray Photon Counting Chip

X-Rays strike an external detector. Generated charge is amplified, discriminated, and counted by this chip and the counter values are read out through a digital interface. 2.2mm x 3.6mm, 0.6um CMOS. Very low power and low noise.

256 Channel X-Ray pulse detection and measuring

X-Rays strike a detector mounted directly to the surface of this chip. Each pixel amplifies the input charge, filters the signal, and measures the amplitude. Digital circuits control the readout of the results. 8.6mm x 9.6mm, CMOS, Low power, very low noise.

Main Features

- 256 channels arranged in a 16x16 matrix at 500um pitch
- Self-resetting charge sensitive amplifiers.
- Maximum count rate above 400E3 photons/s for all channels in parallel
- Gains and offsets of each channel are digitally adjustable.

- Input energy range 1keV – 150keV. Both input polarities.
- Selectable shaper filter shaping time, 1usec – 4usec in 8 steps for noise tradeoff versus detection rate selection.
- Data readout is controlled by a programmable token logic.
- Additional data read options are provided by an 8 bit data bus
- Multiple chips may be used in the same system by daisy-chaining up to 16 chips that share a common analog output. The outputs use tri-state buffers to avoid conflicts.
- A test signal input can be connected to the detector inputs of any channel or combination of channels.
- An analog monitor output can be connected to any channel to display its analog signal.
- The cell token logic ensures that only one peak detect output is put on the analog bus at a time.
- Power consumption: 1500mW nominal
- Input referred noise < 200 e rms.
- Die size: $\approx 8.575 \times 9.535 \text{ mm}^2$ sized to accommodate tight integration of multiple detectors
- Input pad spacing: 0.15 mm to allow 57 pads on one edge of the chip.
- Active low (internally pulled down) chip enable that allows for connecting the data busses of several IC's in parallel.
- All digital inputs and outputs are compatible with standard 3.3V logic (LV or LVDS).

66 & 34 Channel X-Ray photon counting chip

Each channel amplifies and filters incoming pulses of generated charge from X-Ray detectors. Charge pulses are binned into 5 separate categories based on pulse magnitude. On chip counters record number of events within each bin. 10.6mm x 4.2mm, 5.9mm x 3.8mm, CMOS, Low power, high speed, low noise.

256 channel X-Ray photon counting discriminator chips

Each channel amplifies incoming charge pulses which come from detectors mounted directly to the surface of the chip. All three chips use the same preamplifier with different backend discrimination and pulse counting circuits. Shown are the analog version, digital version, and mixed analog/digital version, 8.6mm x 9.6mm each, CMOS, low power

36 Channel X-Ray photon detection and measurement chips

X-Rays strike a detector wire bonded to this chip. Each pixel amplifies the input charge, filters the signal, and measures the amplitude and detection time. Digital circuits control the readout of the results. 6mm x 6mm each, 2 different CMOS processes (0.5um and 0.6um), very low power, very low noise.

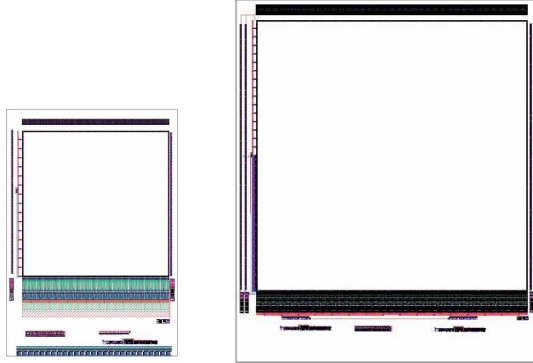
This is a multi-channel X-ray detector readout ASIC designed for multiple applications and many different detector types. This is accomplished with many different programmable features. The unique DC coupling of the channel along with the digital readout circuits allow high duty cycle and detection rates.

Feature	Specification
Signal range	Two full-scale ranges; 56 and 338 ke, selectable for each channel,(9fC and 54fC),(256keV and 1.5Mev)
Input polarity	Selectable channel-by-channel
Number of channels	34 complete + 2 for test and characterization
Input Referred Noise	150 e- rms
Noise optimization for detector capacitance	2 pF and 9 pF detector capacitance
DC leakage current	+/- 5nA maximum
Power consumption	~7mW per channel with all features, adjustable
Fast timing output	Jitter minimized
Channel-to-channel time difference	Implemented
Trigger comparator thresholds	Individually adjustable by internal 8 Bit DACs for each channel
Peaking times	0.1us to 4us + 40us in 16 steps
High count rates	Using pole zero cancellation, capable of over >200,000 counts per second with digital readout system.
Detector structure	Heterogeneous or homogeneous
Key gamma signals	14 keV, 60 keV, 141 keV, 511 keV, 662 keV, up to 1.33 MeV
System components	Pipeline A/D converter, FPGA state machine controller, data FIFO
Interface	Minimum pin count and support component count
Readout mode	Maximum flexibility through hit register
Deadtime per event	<5us for digital interface

CCD Imager for Mammography (currently in testing phase)

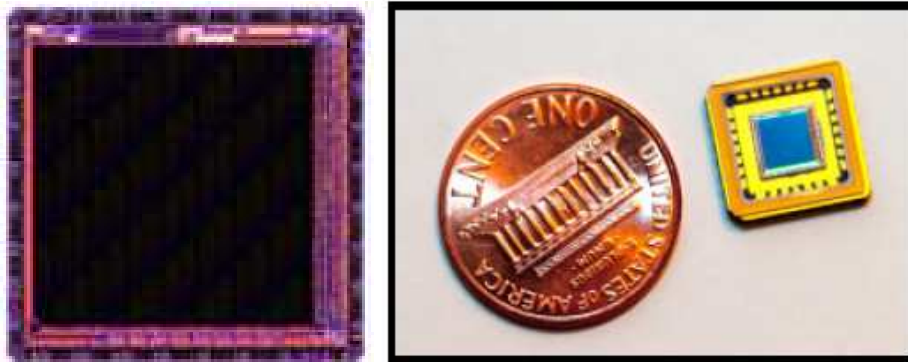
Very large CCD chip 21mm x 12.5mm

128 x 128 & 256 x 256 IR Photodetection array



Each pixel measures the current through bolometric sensor. The results are multiplexed onto a serial analog output for use in a IR imaging system. 7mm x 11mm & 13mm x 16mm, CMOS

328 x 328 Visible Imager

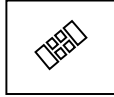


This imager chip is a CMOS detector array with built in offset cancellation. The output is a proprietary digital serial or parallel format. 5.1mm x 5.1mm CMOS, low power.

SemQuest recently finished the design and preproduction phases of this imager with these approximate specifications.

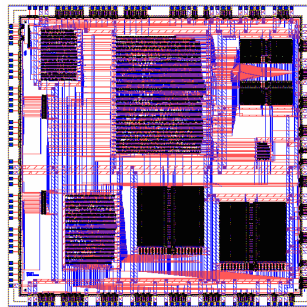
- Relatively large pixels for high sensitivity and good image quality for use with low cost and simple optics.
- Low cost per packaged and tested part at low volume, (\$10 & 20,000 parts per year)
- Selectable window size
- High speed readout for fast frame rate (100 fps)
- Programmable serial interface

Optical Disk Read head 1 & 2



Detector chips for optical disk read head. SemQuest performed layout only. CMOS.

32 Channel triggering detection ASIC



Optical detectors are coupled to the analog inputs of this chip. When a programmable analog threshold is exceeded, this chip prioritizes the event and sends digitally encoded events to a proprietary system., 16.1mm x 16.1mm CMOS